INSTRUCTION MANUAL

KX09A
MEMORY PROTECTION OPTION

PDP-9

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

DEC-09-I1BA-D

KX09A

MEMORY PROTECTION OPTION

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CHAPTER 1
INTRODUCTION

The KX09A Memory Protection Option is a PDP-9 computer option manufactured by Digital Equipment Corporation. It is used to trap certain instructions, references to protected areas of the core memory and references to nonexistent memory banks. This document and the referenced documents provide information necessary for installation, operation and maintenance of the KX09A Memory Protection Option. The level of discussion assumes that the reader is familiar with the core memory system of the PDP-9 central processor.

1.1 RELATED DOCUMENTATION

The documents listed in Table 1-1 contain material which supplements information in this document.

Table 1-1
Reference Documents

Title	Document Number	Contents
Digital Logic Handbook	C-105	Specifications and descriptions of most FLIP CHIP * modules, plus simplified explanation of the selection and use of these modules in numerous applications.
PDP-9 User Handbook	F-95	Operation and programming information for the PDP-9.
PDP-9 Maintenance Manual Volumes I and II	F-97	Operation and maintenance information for the PDP-9, including engineering drawings.
DM09A Instruction Manual	DEC-09-19AB-D	Operation and maintenance information for the PDP-9 DMA Multiplexer option.
KX09A Memory Protect Test	MAINDEC-9A-D1EB-D	Operating instructions and program listing for the KX09A diagnostic program.

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1.2 SYSTEM DESCRIPTION

The KX09A Memory Protection Option is connected to the PDP-9 central processor and control memory system (Figure 1-1). It establishes a foreground/background environment for PDP-9 time-sharing processing activity by specifying the boundary between the protected (lower) and unprotected (upper) regions of core memory. Memory locations are assigned to the protected region in increments of 2000_8 locations and the protected region is variable by a programmed instruction.

All instructions are monitored before they are executed. The logic within this equipment traps instructions that reference locations below the boundary or instructions that are in the illegal category. This trapping causes the execution of an effective JMS instruction after the machine cycle in which the attempted violation occurred. The address referenced by the effective JMS instruction will be location absolute 20 if the program interrupt facility is disabled, or location absolute 0 if the program interrupt facility is enabled.

If a nonexistent memory bank is referenced by an instruction, a trap occurs to prevent a hang-up condition in the central processor.

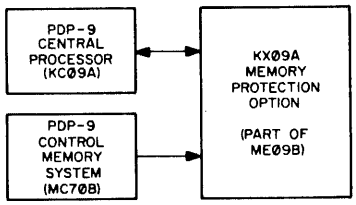


Figure 1-1 Memory Protection System

CHAPTER 2
INSTALLATION

The KX09A Memory Protection Option consists of 47 FLIP CHIP modules of the B-, R-, S- and W-series mounted in two Type 1943D module mounting panels. Wiring for the KG09A, MP09A and MP09B options is also installed on the two module mounting panels. The complete assembly, Type ME09B, is mounted in two spaces immediately above the paper tape reader/punch unit in the PDP-9 central processor cabinet. There are no special installation requirements other than those required for the PDP-9 central processor if the equipment is installed in the plant. If a field installation is performed, insert the module complement per drawing D-MU-KX09-A-1. Remove jumpers and install external components using drawing A-CP-ME09-B-3 as a reference.

2.1 INTERCONNECTIONS

Standard PDP-9 I/O bus cables and three flexiprint cables connect the KX09A to the PDP-9 central processor, and three flexiprint cables complete the connections to the control memory system. The I/O bus cables are shown on drawing D-IC-KX09-A-4 and the six flexiprint cables are shown on drawing D-IC-KX09-A-5, sheet 1. Drawing D-IC-KX09-A-5, sheet 2, shows a schematic view of the installed cables and identifies the cable lengths and the terminating module types.

2.2 POWER REQUIREMENTS

The KX09A draws the necessary dc power from the PDP-9 central processor power buses. It requires 10V at 0.2A and -15V at 3.2A.

2.3 ENVIRONMENT

The environmental specifications for the KX09A are identical to the PDP-9 central processor environmental specifications.

2.4 ON-SITE CHECKOUT

Check wiring for shorts and correct any shorts that are found. Check that the jumpers for the KX09A are removed from W18-D25 and that all unused pins on W18-D25 are jumpered per drawing A-CP-ME09-B-3. Check that the external components are installed. Check all cables using drawing D-KX09-A-5 (sheet 2) as a reference. Check that the jumper between H35C and H35F (USER MODE (1)B to ground) in the PDP-9 central processor is removed.

Turn on power and run a few small programs to check the operation of the boundary register and the PRTCT switch. A sample program is shown below:

```
LAS
LBR
JMP.-2
```

The boundary register should follow the state of the appropriate bits in the data switches. If the results are incorrect, check the IOT's and the logic for missing signals, etc.

Run a JMP. program. Press the START key with the PRTCT switch in the UP position and observe that both the USMD indicator and the indicator above the PRTCT switch illuminate. Check that the PRTCT switch has no further effect once the program is running. Check that the IO RESET key clears the boundary register and the USMD lights.

Run the diagnostic program MAINDEC-9A-D1EB-D and run margins on racks A, B, C, and D of the ME09B using margins of 10 ± 4V and -15 ± 3V.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 OPERATION

The user mode (memory protect) of the KX09A is enabled by either a MPEU instruction, or by placing the PRTCT switch on the PDP-9 operator console in the UP position and pressing the START key. Once the program has started, the KX09A is in user mode and the PRTCT switch has no further effect. The indicator above the PRTCT switch lights when the user mode is enabled.

3.1.1 KX09A Indicators

The indicators shown in Figure 3-1 are mounted above the PDP-9 marginal check panel. Indicator functions are listed in Table 3-1.

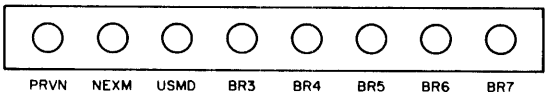


Figure 3-1 KX09A Indicator Panel

Table 3-1
KX09A Indicators

Name	Function
PRVN	Lights when protect violation flag is raised.
NEXM	Lights when nonexistent memory flag is raised.
USMD	Lights to indicate that the user mode is enabled.
BR3 through BR7	Indicate the upper limit (in 2000_8 increments) of the protected region of core memory.

3.2 PROGRAMMING

The KX09A memory protection option adds the IOT instructions listed in Table 3-2.

Table 3-2
KX09A IOT Instructions

Mnemonic	Octal Code	Function
MPSNE	701741	Skip on nonexistent memory flag. The nonexistent memory flag is set whenever the processor attempts to reference a nonexistent area of core. For a 32K machine, the flag would never get set.
MPSK	701701	Skip on violation flag. The memory protect violation flag will be set whenever the execution of an instruction has violated the provision of memory protection.
MPEU	701742	Enter user (protect) mode. Memory protect mode will be entered at the end of the next instruction that is not an IOT.
MPCV	701702	Clear violation flag.
MPCNE	701744	Clear nonexistent memory flag.
MPLD	701704	Load the memory protection boundary register with the contents of AC3 through 7. The boundary register will store the number of 2000_8 word blocks to be protected.

3.2.1 Stored Data Word Format

Figure 3-2 shows the data format of the word deposited in location 20 or 0 when a violation is trapped.

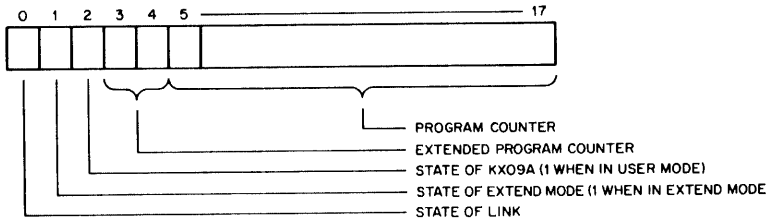


Figure 3-2 Stored Data Word Format

CHAPTER 4
THEORY OF OPERATION

4.1 BLOCK DIAGRAM DISCUSSION

The KX09A Memory Protection Option (Figure 4-1) establishes a foreground/background environment for PDP-9 time-sharing processing activity by specifying the boundary between protected (lower) and unprotected (upper) regions of the core memory. Memory locations are allocated to the protected region in word blocks of 2000_8 locations. A number that represents the upper limit of the protected region is transferred from the PDP-9 AC register and to the boundary register via the IO BUS 03 through 07 lines. This number is jammed into the boundary register by an MPLD instruction.

The KX09A can be placed in the user (protect) mode by an MPEU instruction or by placing the PRTCT switch in the UP position and pressing the START key on the PDP-9 operator console. With the user mode enabled, the KX09A monitors the instruction to be performed for illegal instructions (instructions that should not be used by time-sharing users; e.g., IOT, OAS, HLT, a chain of XCT), references to memory locations within the protected region, and reference to nonexistent memory banks. If one of these conditions is detected, control is transferred to a monitor program before the instruction is executed.

These functions are performed in the following manner. A comparator circuit compares the number stored in the boundary register with bits 3 through 7 of the instruction address. The KMA < BR signal is generated and the monitor circuit is enabled if the number in bits 3 through 7 is less than the number in the boundary register. The operation code of the instruction is decoded in the monitor circuit and the monitor circuit is enabled if the instruction is in the illegal category. To check for references to nonexistent memory banks, the MEM START pulse sets the MEM OK flip-flops and the MEM STROBE pulse clears the flip-flop. If a nonexistent memory bank is referenced, the MEM STROBE pulse is not generated and the MEM OK flip-flop remains set. Then, the next CLKD pulse sets the NON-EX MEM flip-flop. Outputs from the MEM OK and NON-EX MEM flip-flops are ANDed enabling the monitor circuit.

When the monitor circuit is enabled, the 1 → FOUND 1 signal is sent to the trap circuit causing the 13 → CMA and FOUND 1 SAVE (B) signals to be generated. The FOUND 1 SAVE (B) signal from the trap circuit is sent to the central processor and causes the execution of an effective JMS instruction after the machine cycle that attempts to violate. The address referenced by the effective JMS instruction is location absolute 20, if the PI facility is disabled, or location absolute 0, if the PI facility is enabled. The 13 → CMA signal sets the PROTECT VIOLATION flip-flop, disables the user mode enable circuit, and sets the CMA register to 33.

The state of the KX09A (a 1 for the user mode) is stored in bit 2 of the storage word by those operations that save the state of the machine (CAL, JMS, PI). The stored program count (PC) will contain one more than the location of the violating instruction, except for JMP to a protected area. In this case, the stored PC will contain the protected address.

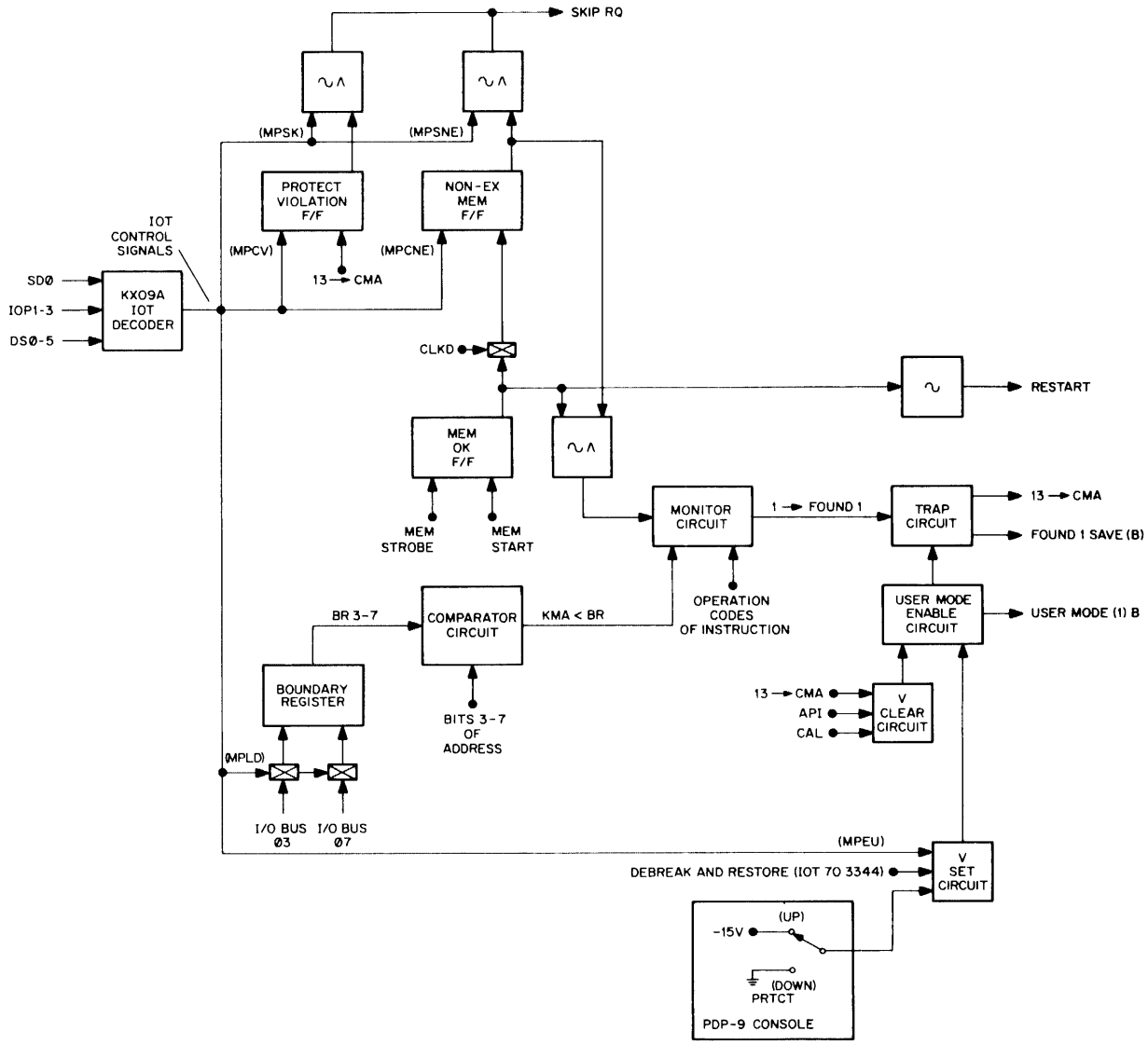


Figure 4-1 Block Diagram

If the user mode is enabled when an API break starts and the API channel address contains a HLT, OAS, or IOT instruction rather than the normal JMS instruction, the instruction is inhibited, the user mode is disabled and no violation is detected. A debreak and restore (DBR) instruction (703344_8) is performed to return the KX09A to the user mode.

A CAL instruction disables the user mode and never causes a violation.

If the user mode is disabled when reference to a nonexistent memory bank is made, the NON-EX MEM flip-flop is set but no trap occurs. Since the MEM STROBE pulse is not generated, the program will hang-up. To prevent this, the output from the MEM OK flip-flop is inverted and sent to the PDP-9 as a RESTART signal (drawing KC-16). The input to B104-F31T is conditioned and the next CM CLK pulse enables the strobe logic. The program continues after a 1 μs pause.

There are six IOT instructions added for the KX09A. The functions of the MPLD and MPEU instructions have been briefly explained in this discussion. Refer to Section 4.3 for complete details on all KX09A IOT instructions.

4.2 DEVICE SELECTION

Signals on the device selection lines (DS0 through DS5) and one subdevice select line (SD0) of the PDP-9 I/O bus are used to select the KX09A Memory Protection Option and generate the required control signals. A description of device selection using drawing D-BS-KX09-A-2 (sheet 1) as a reference follows.

Device select lines DS0 and DS1 are inverted generating buffered signals. These signals and the signals on DS2 through DS5 are sent to a W103 module that has been coded for a 17_8 code. The signal on the SD0 line is inverted generating complementary SD0 signals. When an KX09A IOT instruction is placed on the I/O bus, the 17_8 code is decoded by the W103 module and enables the IOP pulse. The resultant IOT pulse is ANDed with the appropriate SD0 signal to generate the control signal.

4.3 INSTRUCTION DESCRIPTIONS

There are six IOT instructions which initiate action in the KX09A Memory Protection Option. The functions performed by these IOT instructions are described below using drawing D-BS-KX09-A-2 (sheets 1 and 2) as a reference.

4.3.1 Skip on Nonexistent Memory Flag (MPSNE): 701741_8

This instruction checks the condition of the NON-EX MEM flip-flop. A -3V level is applied to R111-A27E if a nonexistent memory bank has been referenced. The signal on the SD0 line (-3V during this instruction) is inverted twice and applied to R111-C28E. The signals on the device selection lines and the IOP1 line are decoded by the W103 decoder module and the resultant pulse is applied to R111-C28D. The AND gate is enabled and its output signal is applied to W640-C29D generating the MPSNE pulse. The MPSNE pulse is applied to R111-A27D generating a skip request (SKIP RQ) that is sent to the PDP-9 via the I/O bus.

4.3.2 Skip on Violation Flag (MPSK): 701701_8

The condition of the PROTECT VIOLATION flag flip-flop is checked with this instruction. A -3V level is applied to R111-A28E if a violation is detected (i.e., a reference to locations below the boundary, an illegal instruction, etc.) and the PROTECT VIOLATION flip-flop is set. The signal on the SD0 line (0V during this instruction) is inverted and applied to R111-D28E. Signals on the device select lines and the IOP1 pulse are decoded by the W103 module and the resultant pulse is applied to R111-D28D. The AND gate is enabled and its output pulse is applied to W640-C29K generating the MPSK pulse which is applied to R111-A28D generating a SKIP RQ.

4.3.3 Enter User Mode (MPEU): 701742_8

This instruction is performed to place the KX09A in the protect (user) mode. The signal on the SD0 line (-3V during this instruction) is inverted and applied to S202-C32V conditioning the DCD gate at the set side of the PRE-USER MODE flip-flop. The signals on the device select lines and the IOP2 pulse are decoded by the W103 module generating the IOT 1702 pulse.

The IOT 1702 pulse is applied to S202-C32U setting the PRE-USER MODE flip-flop and applying -3V to R111-D32E. During this instruction and all IOT instructions, the IOT flip-flop in the PDP-9 (drawing KC12) is set. Therefore, 0V is applied to R111-D32D, disabling the DCD gate at the set side of the USER MODE flip-flop. The DCD gate remains disabled until an instruction other than an IOT instruction is performed. Then, the IOT flip-flop is cleared, R111-D32D goes to -3V, the DCD gate is enabled and the USER MODE flip-flop is set by the DONE (1) pulse at the end of the instruction. A 0V level from the USER MODE flip-flop is inverted generating the USER MODE (1)B signal that is sent to the central processor as UM (1) via the memory extension/parity interface (drawing KC-28).

4.3.4 Clear Violation Flag (MPCV): 701702_8

The PROTECT VIOLATION flip-flop (violation flag) is cleared by this instruction. The signal on the SD0 line (0V during this instruction) is inverted twice and the resulting signal is applied to S202-B29L conditioning the DCD gate at the clear side of the flip-flop. Signal IOT 1702 is generated by the W103 decoder module and applied to S202-B29K clearing the flip-flop.

4.3.5 Clear Nonexistent Memory Flag (MPCNE): 701744_8

This instruction is performed to clear the NON-EX MEM (nonexistent memory flag) flip-flop. The signal on the SD0 line (-3V during this instruction) is inverted and applied to the DCD gate at the

clear side of the NON-EX MEM flip-flop. The W103 decoder module generates the IOT 1704 pulse that is also applied to the DCD gate. The DCD gate is enabled and the flip-flop is cleared.

4.3.6 Load the Boundary Register (MPLD): 701704_8

The protected area of core memory is established during the performance of this instruction. A number that represents the number of 2000_8 word blocks to be protected is sent from the AC to the jam inputs of the boundary register flip-flops via I/O bus 03 through 07. The signal on the SD0 line (0V during this instruction) is inverted and applied to R111-D28S. The signals on the device selection lines and IOP4 are decoded by the W103 decoder module and the resultant signal is applied to R111-D28R. The AND gate is enabled and its output signal is applied to a pulse amplifier generating the MPLD (IOT 1704) pulse which enables the jam inputs of the boundary register jamming the number into the register.

The output signals from the boundary register are sent to a comparator circuit at the top of drawing D-BS-KX09-A-2 (sheet 1). Bits 3 through 7 of the referenced address (bits 3 and 4 specify the memory bank number) are also sent to the comparator circuit and compared with the contents of the boundary register. Any reference to a memory location with an address lower than the number contained in the boundary register causes the KMA < BR signal to be generated. Any reference to a location which is equal to or greater than the contents of the boundary register has no effect.

4.4 DETAILED DESCRIPTIONS

The logic contained in the four circuit blocks (Figure 4-1) is described using drawing D-BS-KX09-A-2 (sheet 1 and 2) as a reference. The PDP-9 Maintenance Manual drawing reference conventions are used in this manual to reference PDP-9 engineering drawings.

4.4.1 Comparator Circuit

The comparator circuit consists of nine AND gates which compare bits 3 through 7 of the referenced memory address with the number stored in the boundary register. The number in the boundary register represents the upper limit of the core memory protected region. If BR7 and BR6 equal 1 the first 6000_8 locations are protected, etc. Complementary signals (BR3 (0) through BR6 (1) and BR7 (1)) are sent to the comparator and connected to the AND gates. Bits 5 through 7 of the referenced address are jammed into KMA5 through KMA7 during the fetch cycle as the instruction is being read into the MB and the complementary outputs from the flip-flops are connected to the AND gates. Complementary signals of EMA3 and EMA4 (bits 3 and 4) of the address are also sent to the AND gates if the memory extension control is in use. This ANDing of signals causes the KMA < BR signal to be generated if the referenced address is within the protected region of core memory.

4.4.2 User Mode Enable Circuit

The user mode enable circuit (sheet 2) consists of the PRE-USER MODE flip-flop, the USER MODE flip-flop, and a number of control gates which enable and disable the KX09A user mode. The USER MODE flip-flop is set or cleared by the DONE (1) signal from the central processor depending on the condition of the PRE-USER MODE flip-flop. The IOT (0) signal from the IOT flip-flop in the PDP-9 central processor prevents the generation of the USER MODE (1)B signal until the IOT flip-flop is cleared. Therefore, an IOT instruction that set the PRE-USER MODE flip-flop does not cause a violation.

The PRE-USER MODE flip-flop can be set in any of the following ways: the DCD gate at the set side of the flip-flop is enabled by an MPEU instruction; the direct set input (S202-C32M) is enabled when the START key is pressed, if the PRTCT switch is in the UP position; or the direct set input is enabled by a DBR instruction, if MB02 (1) is 1 (bit 2 of the word deposited in location 20 or 0 when a violation is trapped).

The PRE-USER MODE flip-flop can be cleared in any of the following ways: the EXT (1) and PROG SYNC (1)B signals are ANDed together during a JMS 0; the EXT (1) and API BK RQ (1)B signals are ANDed together during a JMS X; CAL (1) and IRI (0) signals are ANDed together during a JMS 20; the 0 → EPC signal generated during an I/O RESET: or the 13 → CMA signal generated when a violation is detected.

When the USER MODE flip-flop is set, the USER MODE (1)B signal goes to -3V. It is sent to the PDP-9 I/O control (drawing KD-3 (3)) where it is applied to S107-H18S as UM (1). The UM (0)B signal at the output of the inverter goes to 0V and performs the following functions: disables the output from R111- J12H (drawing KD-3 (3)) preventing the IOP pulses from being generated and inhibiting the IOT instruction; prevents data from being loaded into the AC during an input transfer by inhibiting the generation of the OR ACI signal (drawing KC-12); prevents an output transfer from the AR by inhibiting the generation of the IOT OR ARO signal (drawing KC-12); during operate instruction, disables the output from R111-J28H (drawing KC-10 (1)) preventing the RUN (0) signal from going to 0V (the HLT instruction is disabled); and inhibits the generation of the LIO and DASO signals (drawing KC-13) required for an OAS instruction by disabling the output from R111-D07U.

4.4.3 Monitor Circuit

The monitor circuit decodes conditions that cause violations and generates the 1 → FOUND 1 signal. The conditions that cause a violation are the second XCT instructions in a chain of XCT instructions (the first XCT instruction is allowed), a HLT instruction, an OAS instruction, an IOT instruction, a reference to a nonexistent memory bank, or a reference to a memory location within the protected

region. The HLT, OAS, and IOT instructions are totally inhibited when the user mode is enabled. If a HLT or OAS instruction is combined with any other operate group instructions (microprogramming), the other parts of the operate group instruction are performed.

An instruction in the illegal category is detected by decoding the operation code (MB00 through MB04) of the instructions. Then, the EXT (0) conditions a DCD gate at the set side of the JAM VIOLATION flip-flop during a fetch entry and the IRI (0) B pulse sets the flip-flop. The JAM VIOLATION pulse is sent to the instruction decoders and generates the 1 → FOUND 1 signal if an operation code for an illegal instruction is present.

A reference to a nonexistent memory bank is detected by ANDing the MEM OK (1) and NON-EX MEM (1) signals. If both flip-flops are set, the 1 → FOUND 1 signal is generated.

If a memory location within the protected region is addressed, the KMA < BR signal is generated and inverted conditioning a pair of AND gates. One of the AND gates generates the 1 → FOUND 1 signal, if the instruction is a JMP to an address within the protected region (the PCI (1)B signal is -3V), and if the program was not just started by depressing the START key (ADSO (0) signal is -3V). This logic allows a reference to an address within the protected region when the program is started with the START key. The second AND gate generates the 1 → FOUND 1 signal if an address within the protected region is addressed directly (IR4 (0) signal 0V) and if the instruction is not a CAL instruction (CAL (0) signal is 0V). This logic allows an indirect reference within the protected region and the execution of a CAL instruction.

4.4.4 Trap Circuit

The trap circuit consists of the FOUND 1 and FOUND 1 SAVE flip-flops and their associated gates. It is enabled and the 13 → CMA and FOUND 1 SAVE (B) signals are generated if a violation is detected and the user mode is enabled.

The USER MODE (1) and PRE-USER MODE (1) signals are ANDed together; the resulting signal conditions a DCD gate at the set side of the FOUND 1 flip-flop. Then the 1 → FOUND 1 pulse sets the FOUND 1 flip-flop when a violation is detected. The leading edge of the FOUND 1 (1) signal sets the FOUND 1 SAVE flip-flop generating the FOUND 1 SAVE signal that is applied to the level input of the PV flip-flop (drawing KC-12).

The SM flip-flop is set (CMA 24) and the SM1 signal is ANDed with a -3V signal from the FOUND 1 flip-flop generating the 13 → CMA pulse. The 13 → CMA pulse is sent to the direct set input of the CMA 2, 4 and 5 flip-flop (drawing KC-19 (1)) setting the CMA register to 33. The PRE-USER MODE flip-flop is cleared and the PROTECT VIOLATION flip-flop is set by the 13 → CMA pulse. To prevent a second 13 → CMA pulse from being generated, the SM (1) signal is delayed and ANDed with the CLKD pulse generating the MEM START pulse that clears the FOUND 1 flip-flop.

When location 33 is addressed, the IRI flip-flop is set and the IRI (1) signal is applied to the jam input of the PV, CAL and IR flip-flops. With FOUND 1 SAVE present, the PV flip-flop is set and the PV (1) signal disables the SA inputs to the IR clearing the IR. The PV (1) signal is also ANDed with the PIE (1) signal. If the PIE (1) signal is -3V (PI enabled), the level input of the CAL flip-flop is disabled and an effective JMS 0 is performed. If the PIE (1) signal is a 0V (PI disabled), the contents of the IR are decoded (all 0 at this time) and an effective JMS 20 is performed.

Since the FOUND 1 flip-flop was cleared by a MEM START pulse generated during a preceding cycle, the DCD gate at the clear side of the FOUND 1 SAVE flip-flop is conditioned by the FOUND 1 (0) signal. The MEM START pulse generated during this cycle enables the DCD gate and clears the FOUND 1 SAVE flip-flop. With both flip-flops cleared, the trap circuit is ready to check the next instruction.

CHAPTER 5
MAINTENANCE

The maintenance procedures contained in the PDP-9 Maintenance Manual apply to the KX09A Memory Protection Option.

5.1 DIAGNOSTIC PROGRAM

The diagnostic program MAINDEC-9A-D1EB-D checks the KX09A Memory Protection Option for normal operation. All IOT instructions associated with the option are tested and the logic's ability to trap instructions, which can interface with the protected area of memory, is checked. The instructions tested include HLT, OAS, any IOT, and an XCT followed by an XCT. Operation of the boundary register is then checked by allocating protected areas of core memory in segments of 2000_8 locations. During the boundary register tests, the program checks that a protect violation does not occur when the referenced address is equal to the contents of the boundary register. Additional tests are provided in the diagnostic program to check KX09A operation when the PDP-9 is equipped with the KG09A Memory Extension Control option and/or the KF09A Automatic Priority Interrupt option.

5.2 RECOMMENDED SPARES

Table 5-1 lists the modules used in the KX09A. All of these modules with the exception of the W640 module, are used elsewhere in the PDP-9 system. Since it is unnecessary to carry duplicate spare modules, one W640 module is the only recommended spare.

Table 5-1
KX09A Modules

Quantity	Type	Function
1	B104	Inverter
1	B105	Inverter
4	B213	Jam Flip-Flop
1	B310	Delay
5	R002	Diode Network
22	R111	NAND/NOR Gate
5	S202	Dual Flip-Flop

Table 5-1 (Cont)
KX09A Modules

Quantity	Type	Function
3	W005	Clamped Load
1	W103	Device Selector
3	W612	Pulse Amplifier
1	W640	Pulse Output Converter

CHAPTER 6
ENGINEERING DRAWINGS

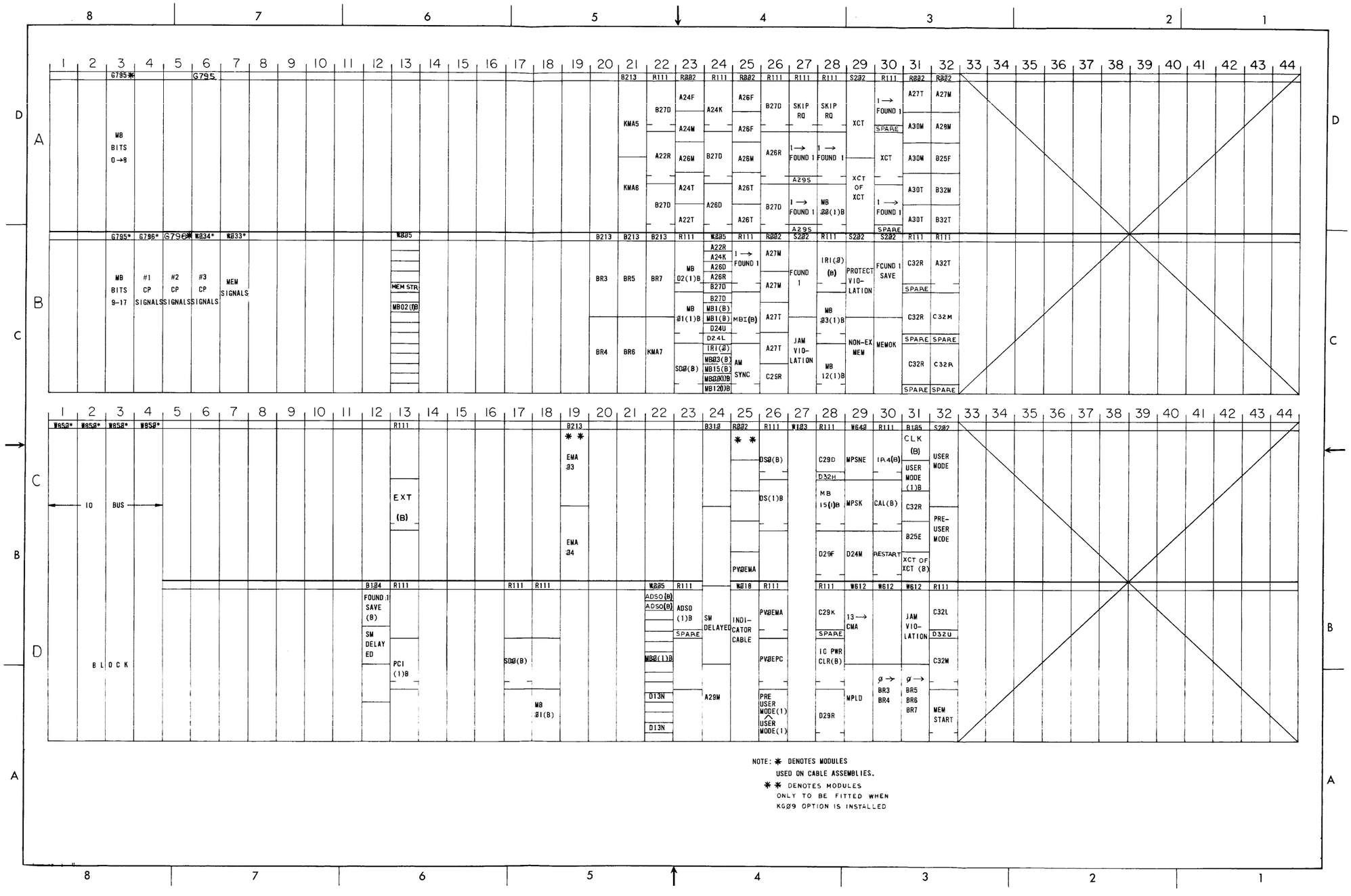
This chapter contains the standard block schematics, circuit schematics, and engineering drawings necessary for understanding and maintaining the KX09A Memory Protection Option. The drawings are listed in the same order as they appear in this manual.

Engineering Drawings

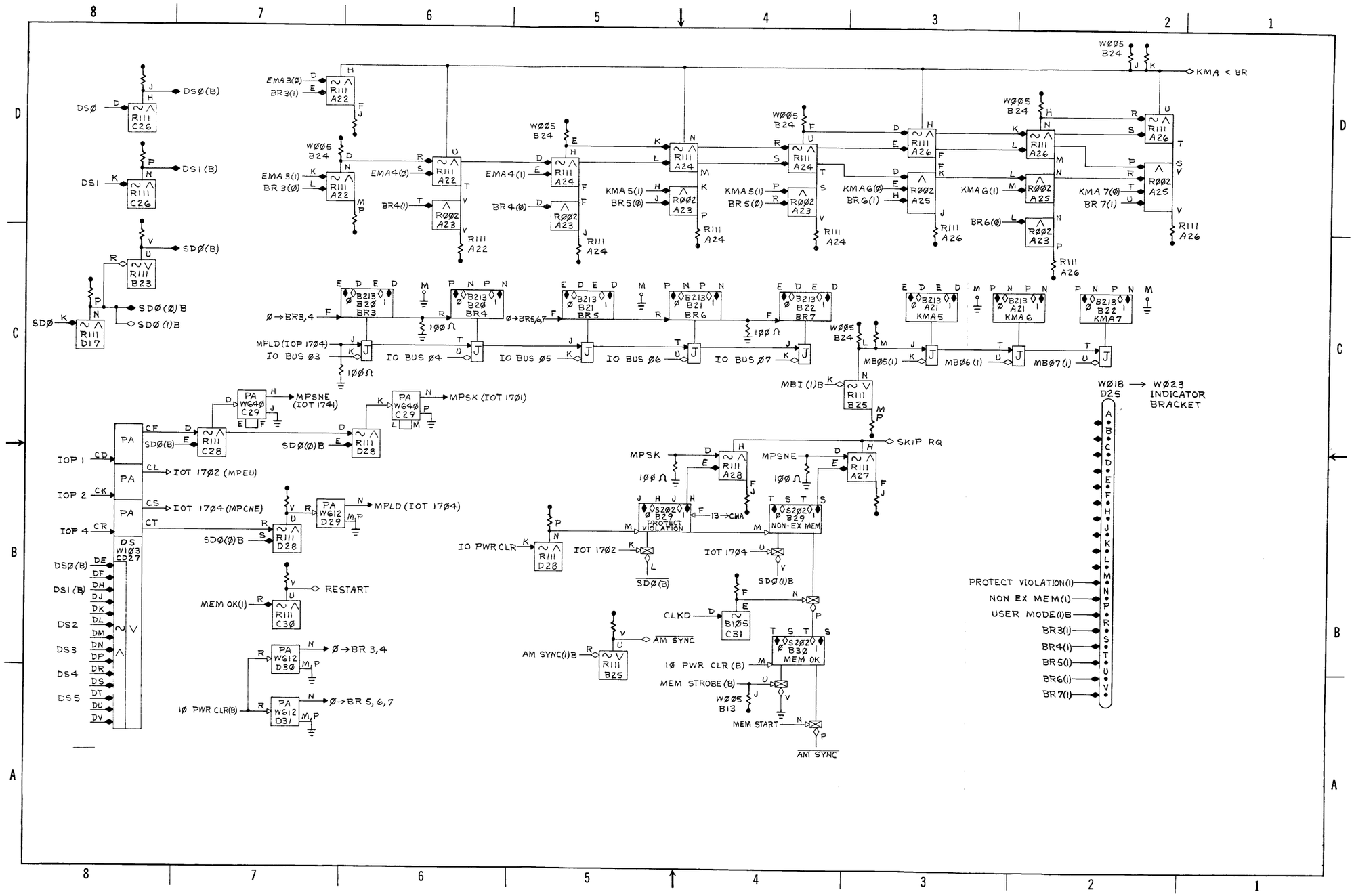
Drawing Number	Title	Revision	Page
D-MU-KX09-A-1	Module Utilization List	A	6-3
D-BS-KX09-A-2	Control (Sheet 1)	A	6-5
D-BS-KX09-A-2	Control (Sheet 2)	A	6-7
D-TD-KX09-A-3	Memory Protect (Sheet 1)	-	6-9
D-TD-KX09-A-3	Memory Protect (Sheet 2)	-	6-11
D-TD-KX09-A-3	Memory Protect (Sheet 3)	-	6-13
D-IC-KX09-A-4	I/O Interface	-	6-15
D-IC-KX09-A-5	Cable Connection Type	B	6-17

Module Schematics

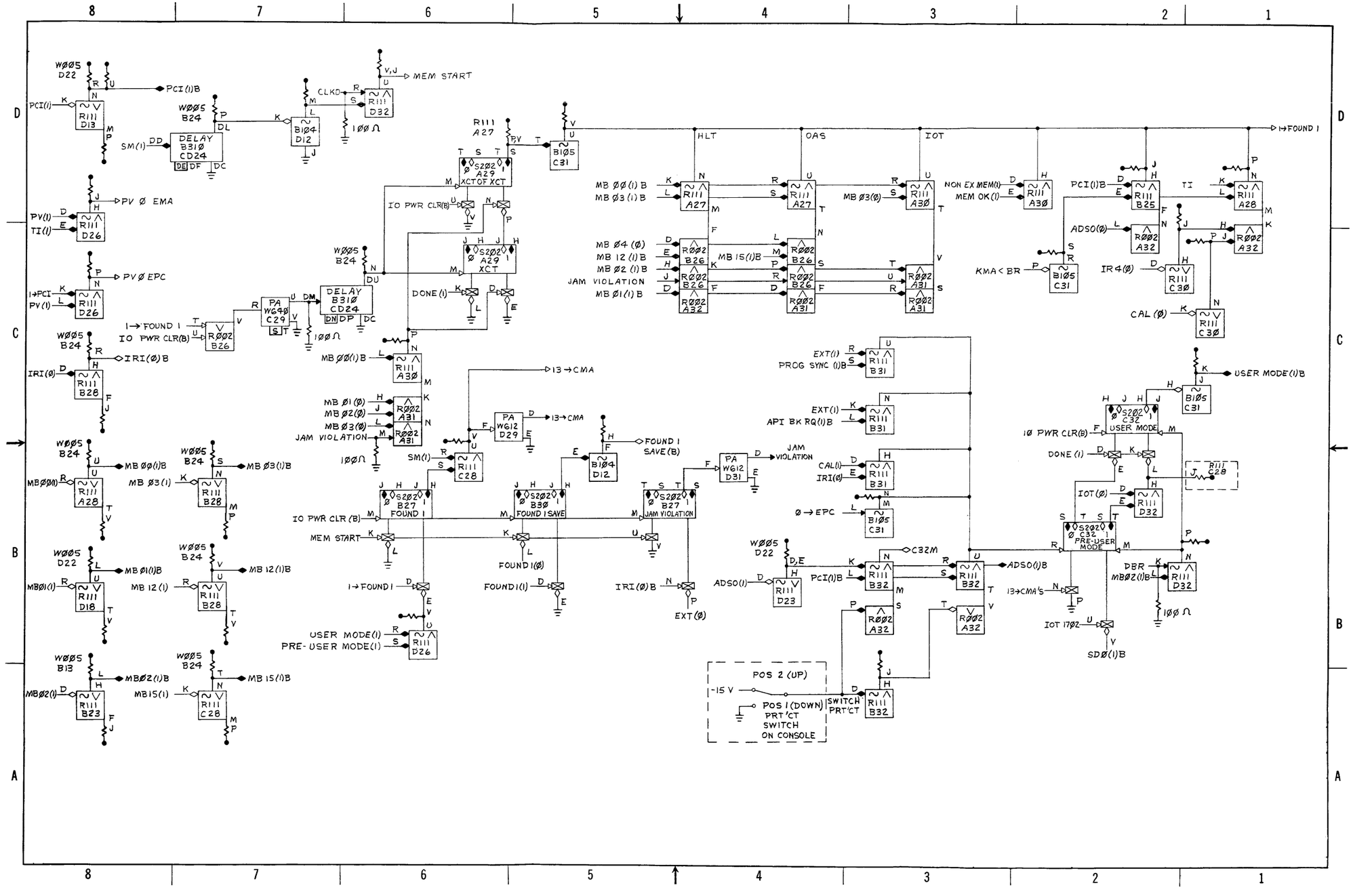
B-CS-B104-0-1	Inverter	C	6-19
B-CS-B105-0-1	Inverter	E	6-19
B-CS-B213-0-1	Jam Flip-Flop	F	6-20
B-CS-B310-0-1	Delay	B	6-20
B-CS-R002-0-1	Diode Network	A	6-21
B-CS-R111-0-1	NAND/NOR Gate	F	6-21
B-CS-S202-0-1	Dual Flip-Flop	D	6-22
B-CS-W005-0-1	Clamped Load	B	6-22
C-CS-W103-0-1	Device Selector	D	6-23
B-CS-W612-0-1	Pulse Amplifier	C	6-24
B-CS-W640-0-1	Pulse Output Converter	L	6-24



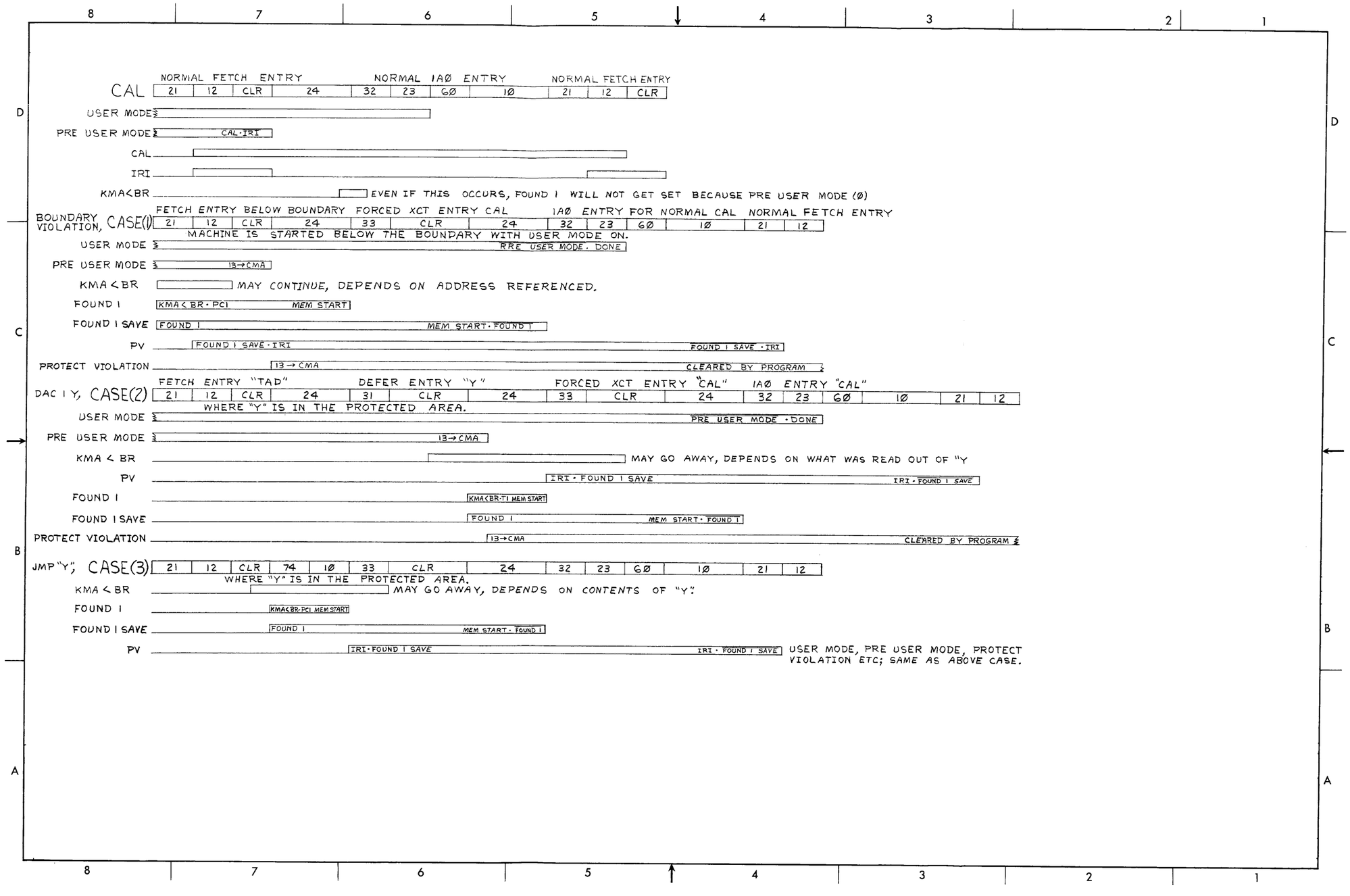
NOTE: * DENOTES MODULES USED ON CABLE ASSEMBLIES.
** DENOTES MODULES ONLY TO BE FITTED WHEN KGØ9 OPTION IS INSTALLED



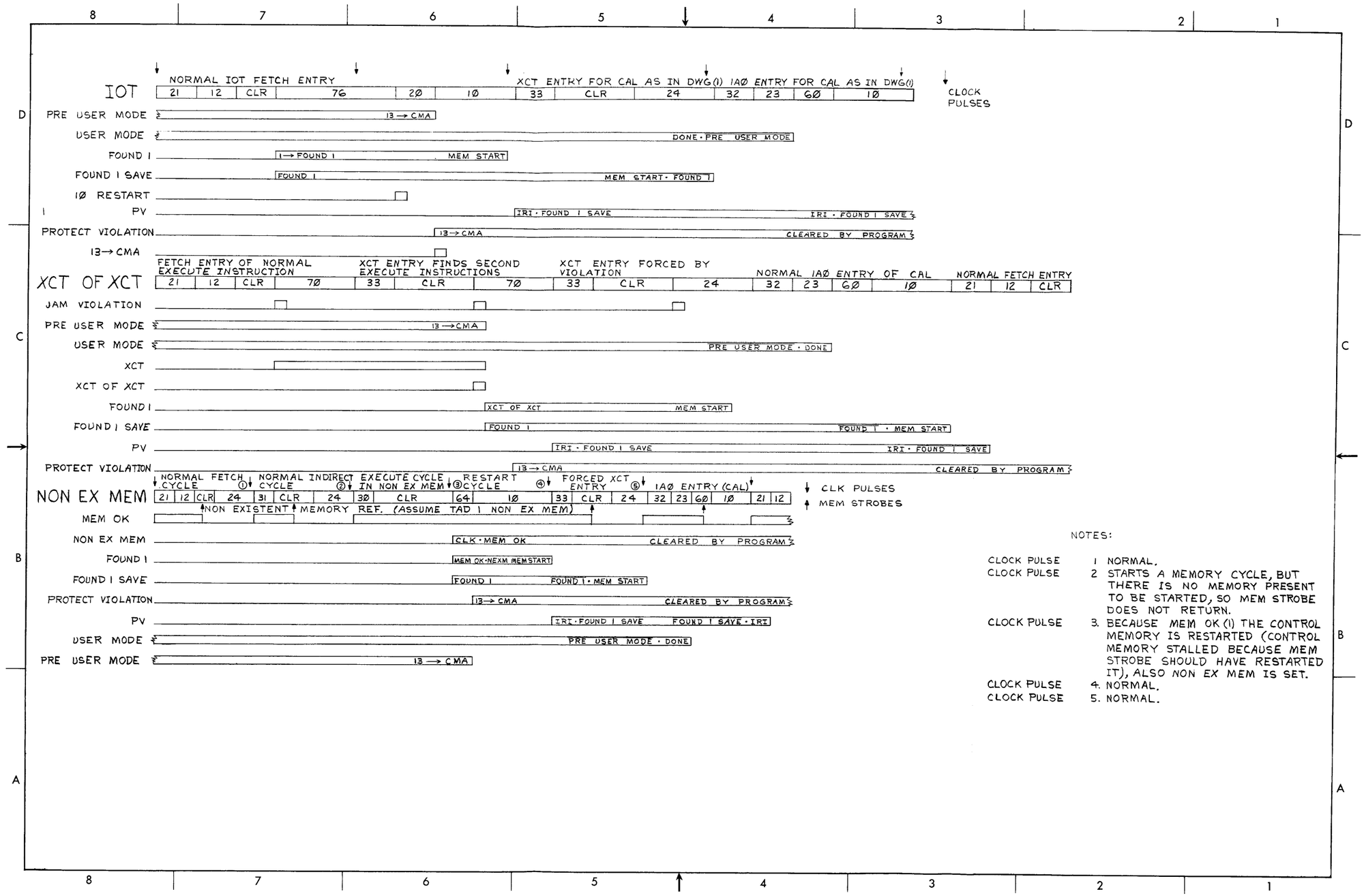
D-BS-KX09-A-2 Control (Sheet 1)



D-BS-KX09-A-2 Control (Sheet 2)



D-TD-KX09-A-3 Memory Protect (Sheet 1)



NOTES:

CLOCK PULSE 1 NORMAL.

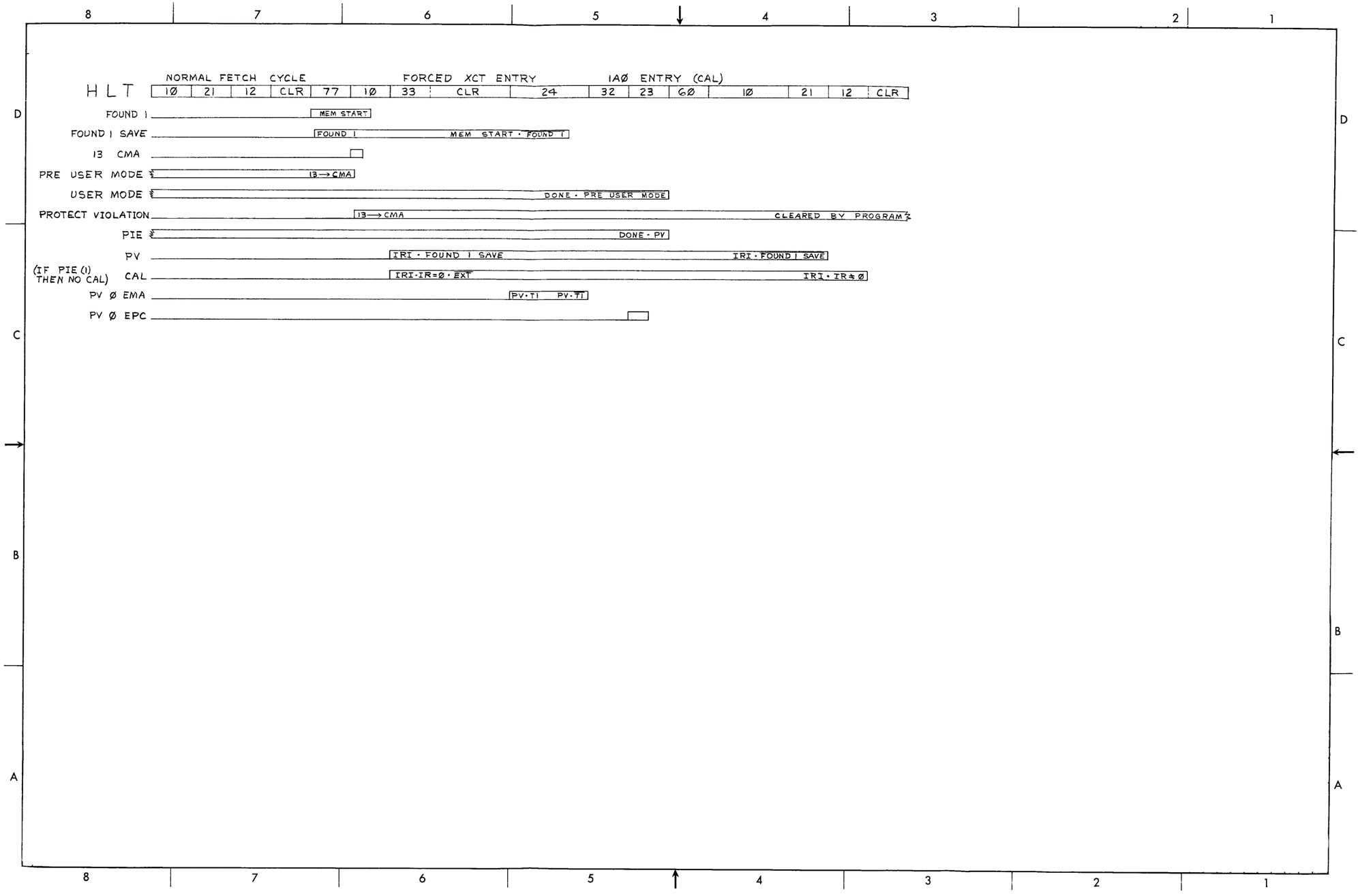
CLOCK PULSE 2 STARTS A MEMORY CYCLE, BUT THERE IS NO MEMORY PRESENT TO BE STARTED, SO MEM STROBE DOES NOT RETURN.

CLOCK PULSE 3. BECAUSE MEM OK (1) THE CONTROL MEMORY IS RESTARTED (CONTROL MEMORY STALLED BECAUSE MEM STROBE SHOULD HAVE RESTARTED IT), ALSO NON EX MEM IS SET.

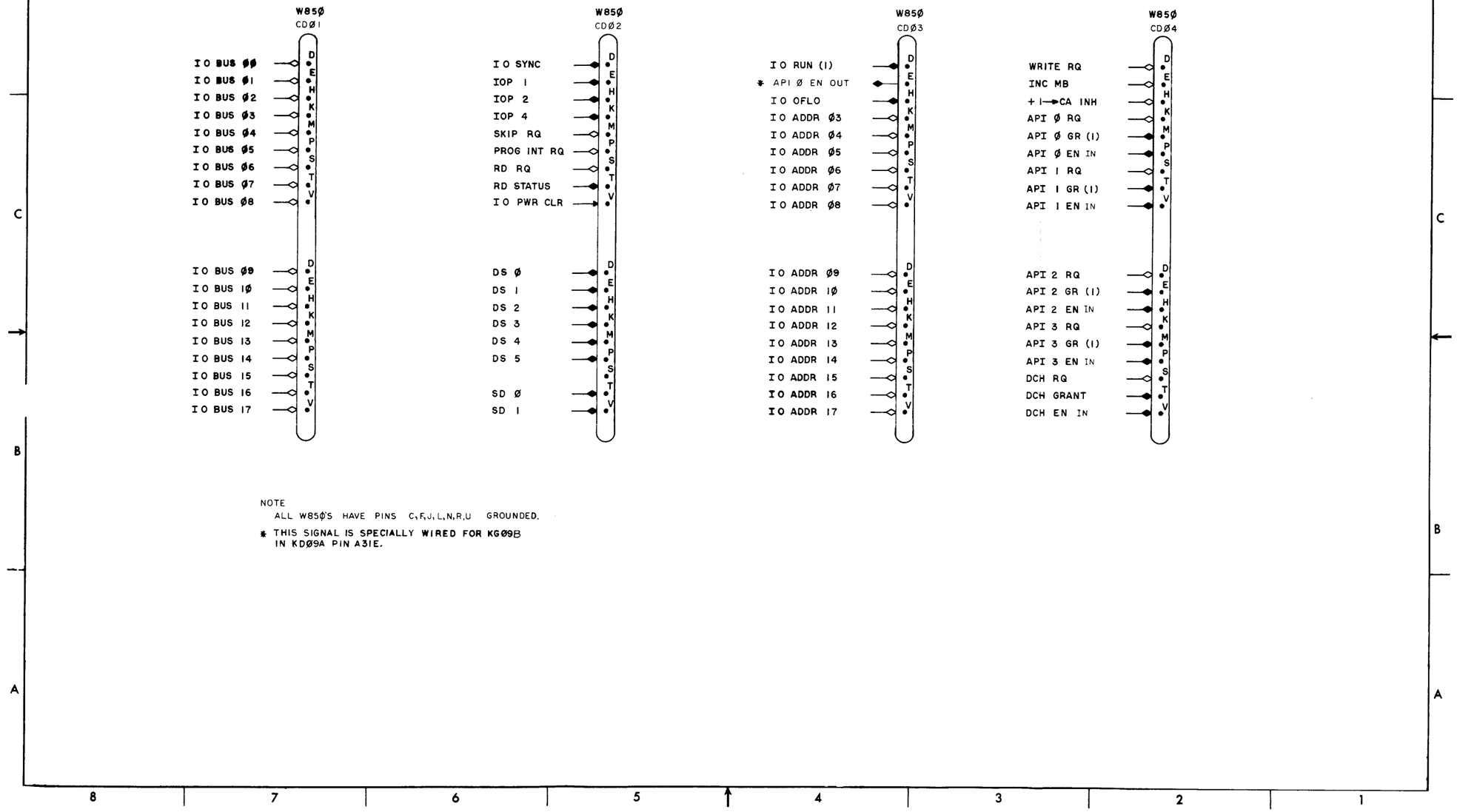
CLOCK PULSE 4. NORMAL.

CLOCK PULSE 5. NORMAL.

D-TD-KX09-A-3 Memory Protect (Sheet 2)



D-TD-KX09-A-3 Memory Protect (Sheet 3)



NOTE
ALL W85Ø'S HAVE PINS C,F,J,L,N,R,U GROUNDED.

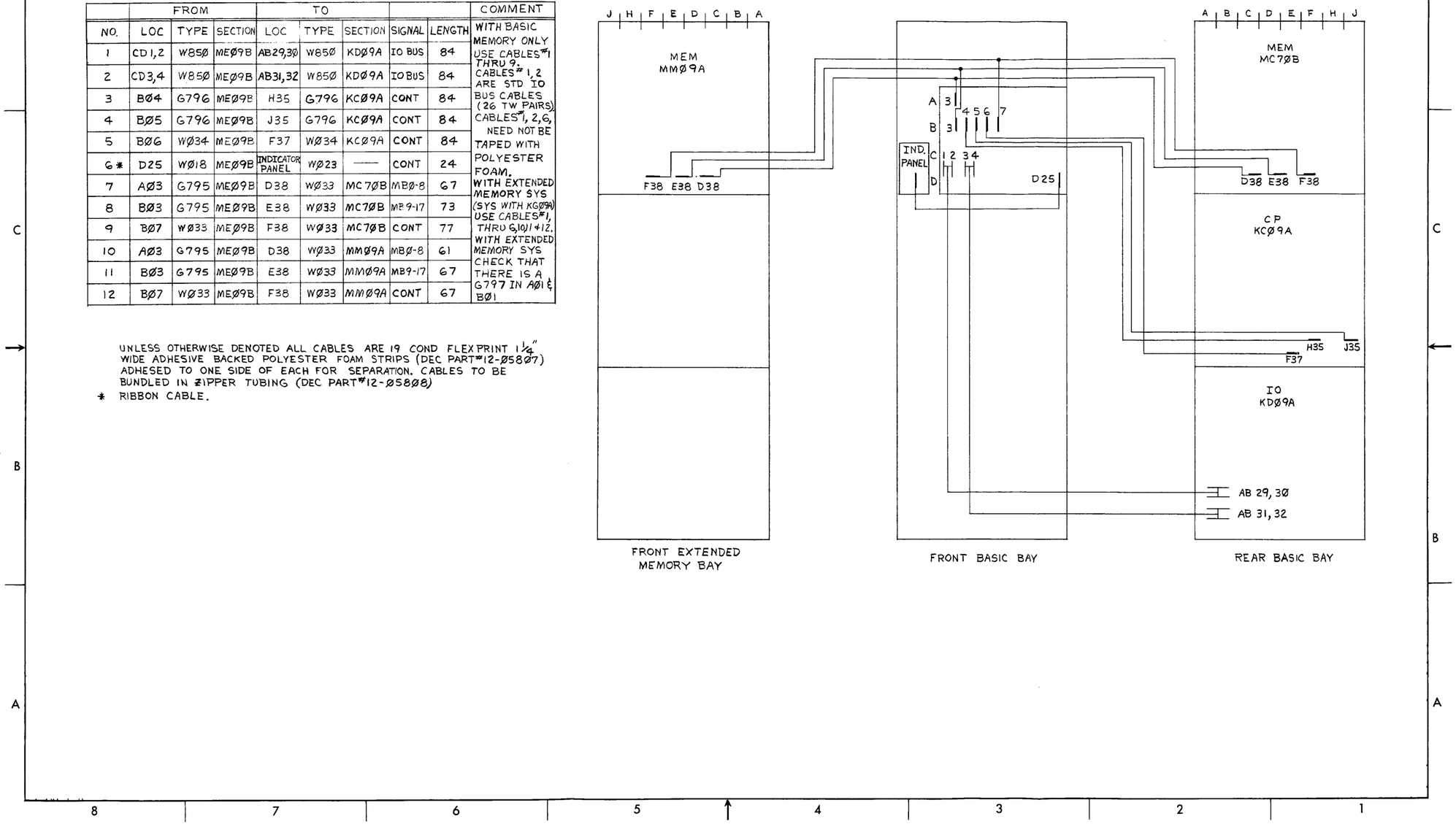
* THIS SIGNAL IS SPECIALLY WIRED FOR KGØ9B IN KDØ9A PIN A31E.

D-IC-KX09-A-4 I/O Interface

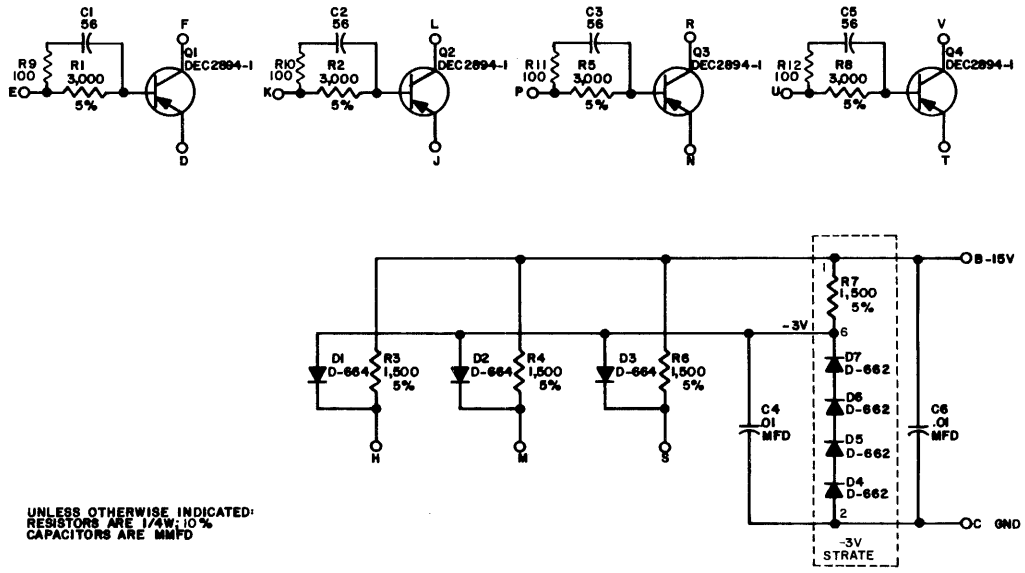
	FROM			TO					COMMENT
NO.	LOC	TYPE	SECTION	LOC	TYPE	SECTION	SIGNAL	LENGTH	
1	CD1,2	W85Ø	ME Ø9B	AB29,3Ø	W85Ø	KD Ø9A	IO BUS	84	WITH BASIC MEMORY ONLY USE CABLES #1 THRU 9. CABLES # 1, 2 ARE STD IO BUS CABLES (26 TW PAIRS). CABLES #1, 2, 6, NEED NOT BE TAPED WITH POLYESTER FOAM. WITH EXTENDED MEMORY SYS (SYS WITH KG Ø9A) USE CABLES #1, THRU 6, 10, 11 & 12. WITH EXTENDED MEMORY SYS CHECK THAT THERE IS A G797 IN A Ø1 & B Ø1
2	CD3,4	W85Ø	ME Ø9B	AB31,32	W85Ø	KD Ø9A	IO BUS	84	
3	BØ4	G796	ME Ø9B	H35	G796	KC Ø9A	CONT	84	
4	BØ5	G796	ME Ø9B	J35	G796	KC Ø9A	CONT	84	
5	BØ6	WØ34	ME Ø9B	F37	WØ34	KC Ø9A	CONT	84	
6 *	D25	WØ18	ME Ø9B	INDICATOR PANEL	WØ23	——	CONT	24	
7	AØ3	G795	ME Ø9B	D38	WØ33	MC 7ØB	MBØ-8	67	
8	BØ3	G795	ME Ø9B	E38	WØ33	MC 7ØB	MB 9-17	73	
9	BØ7	WØ33	ME Ø9B	F38	WØ33	MC 7ØB	CONT	77	
10	AØ3	G795	ME Ø9B	D38	WØ33	MM Ø9A	MBØ-8	61	
11	BØ3	G795	ME Ø9B	E38	WØ33	MM Ø9A	MB9-17	67	
12	BØ7	WØ33	ME Ø9B	F38	WØ33	MM Ø9A	CONT	67	

UNLESS OTHERWISE DENOTED ALL CABLES ARE 19 COND FLEXPRINT 1¼" WIDE ADHESIVE BACKED POLYESTER FOAM STRIPS (DEC PART#12-Ø58Ø7) ADHESED TO ONE SIDE OF EACH FOR SEPARATION. CABLES TO BE BUNDLED IN ZIPPER TUBING (DEC PART#12-Ø58Ø8)

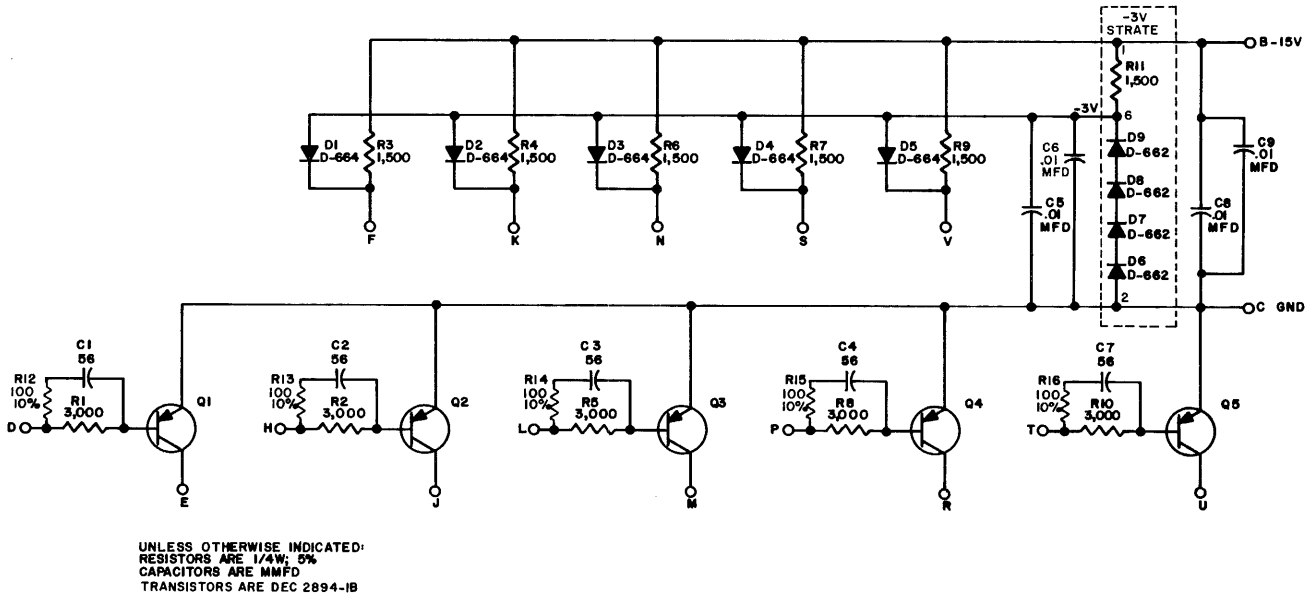
* RIBBON CABLE.



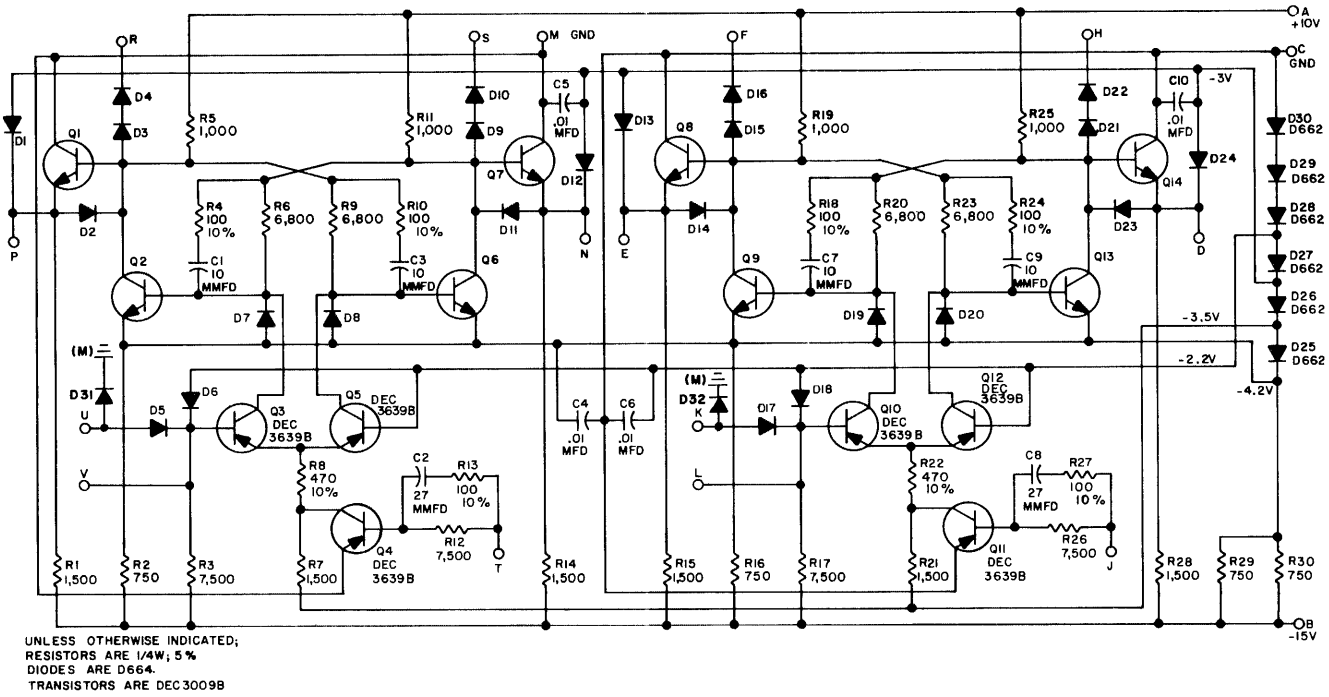
D-IC-KX09-A-5 Cable Connection Type



B-CS-B104-0-1 Inverter

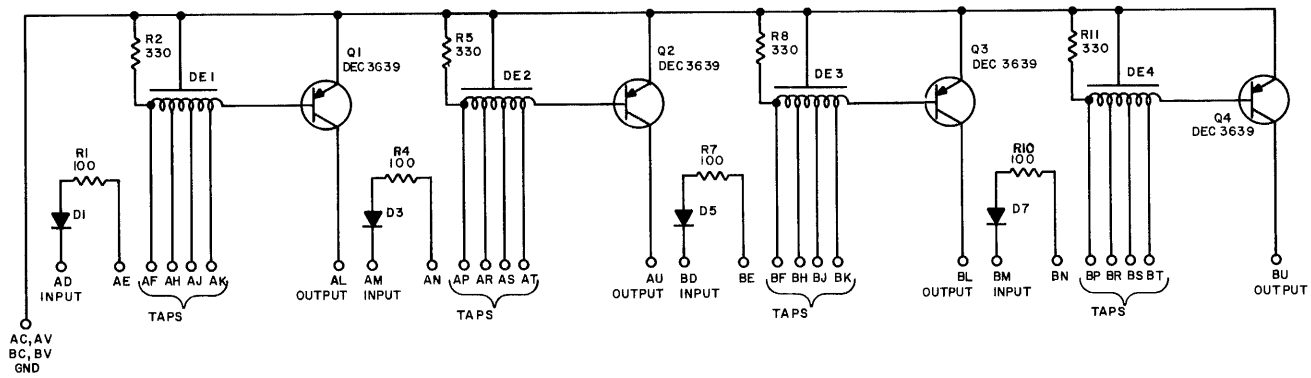


B-CS-B105-0-1 Inverter



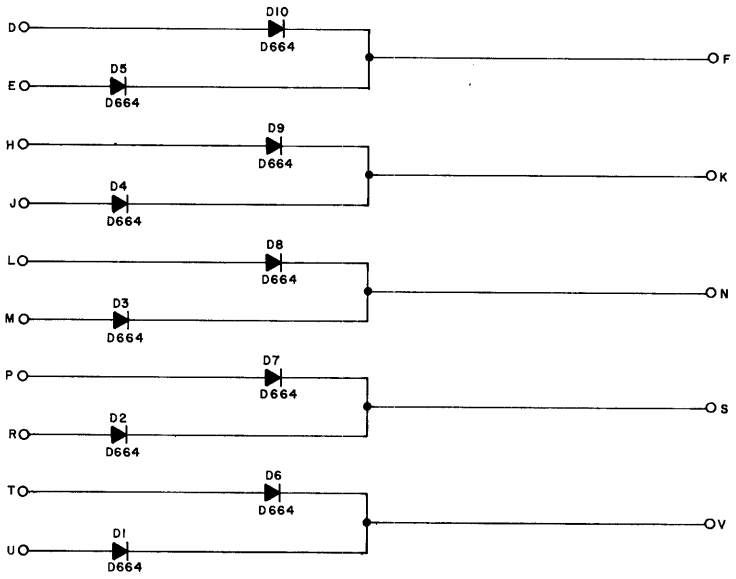
UNLESS OTHERWISE INDICATED;
RESISTORS ARE 1/4W; 5%
DIODES ARE D664.
TRANSISTORS ARE DEC3009B

B-CS-B213-0-1 Jam Flip-Flop

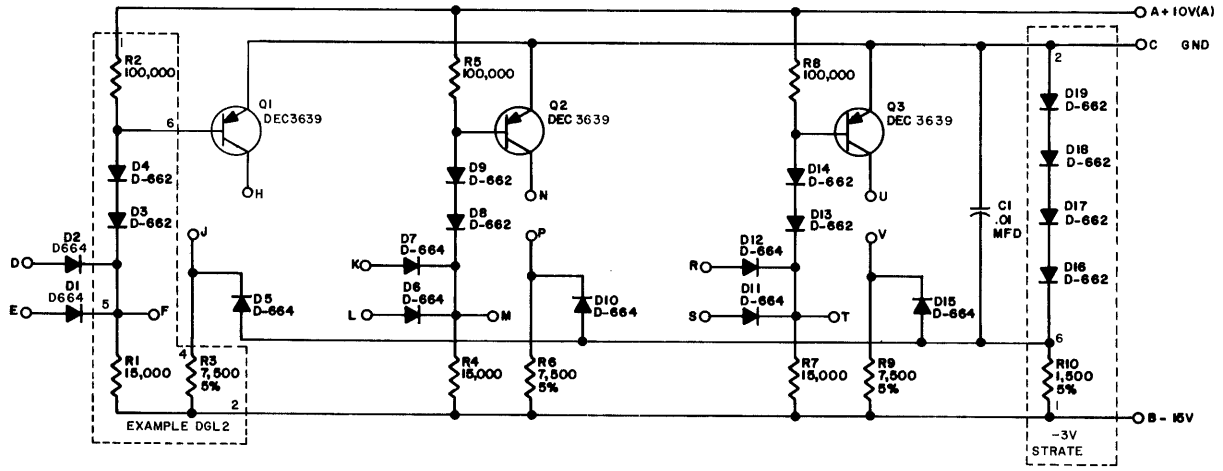


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE D-664
DE1 - DE4 ARE TECHNITROL, .05 usec, 330 Ω TAPS AT .0125 usec, DD-330-5-1, 6012

B-CS-B310-0-1 Delay

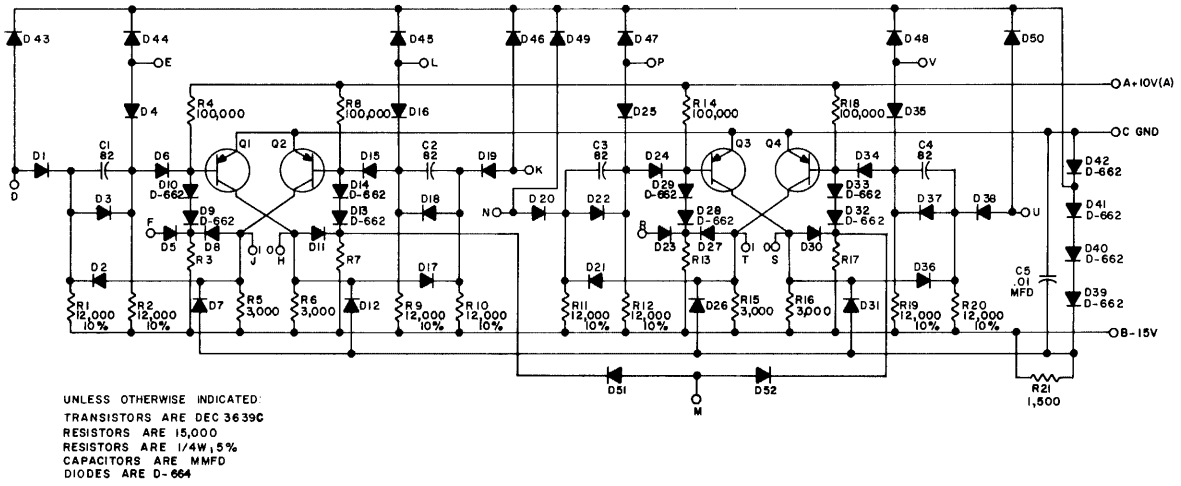


B-CS-R002-0-1 Diode Network

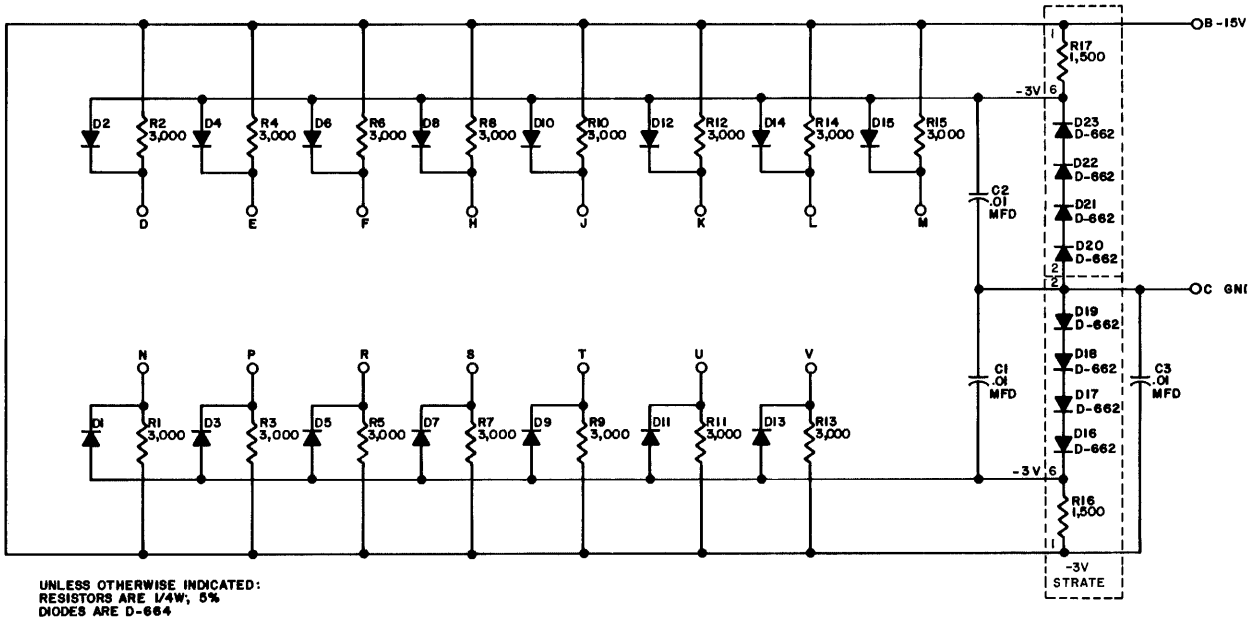


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIB

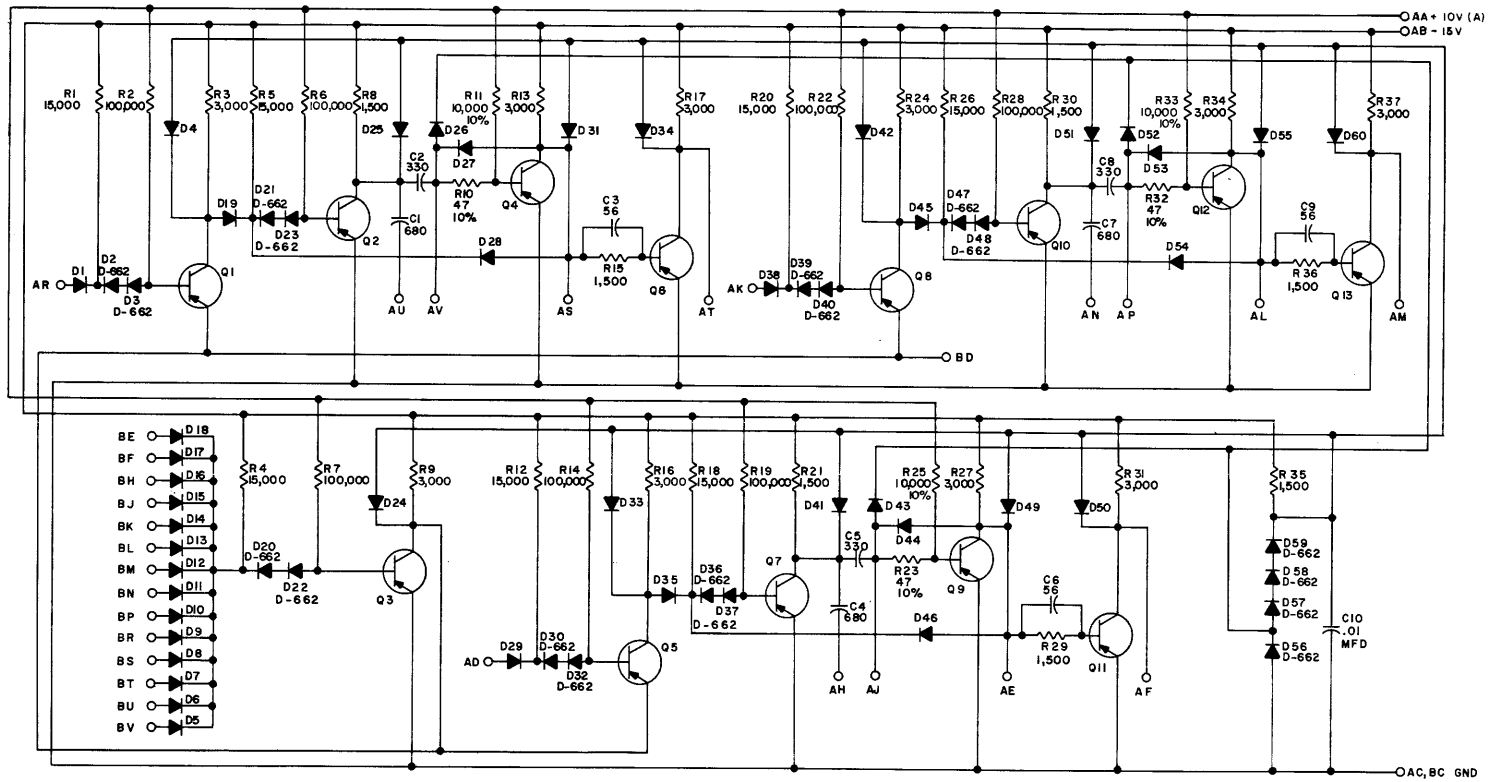
B-CS-R111-0-1 NAND/NOR Gate



B-CS-S202-0-1 Dual Flip-Flop

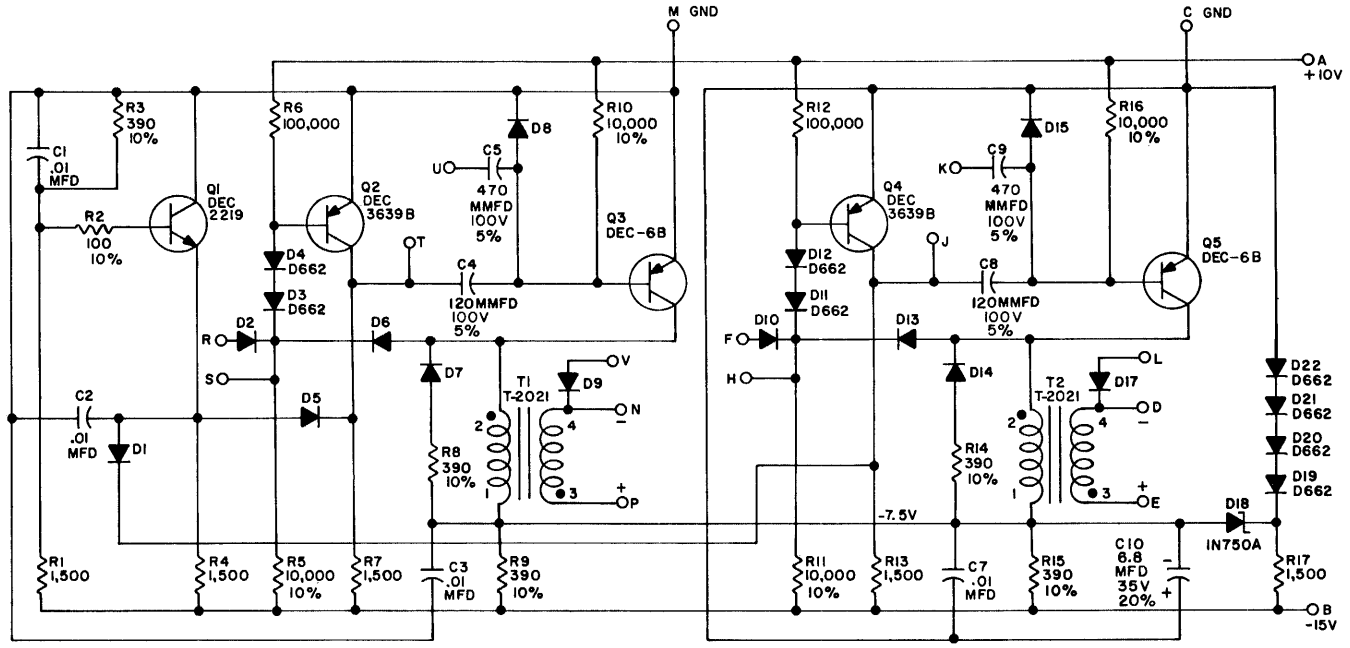


B-CS-W005-0-1 Clamped Load



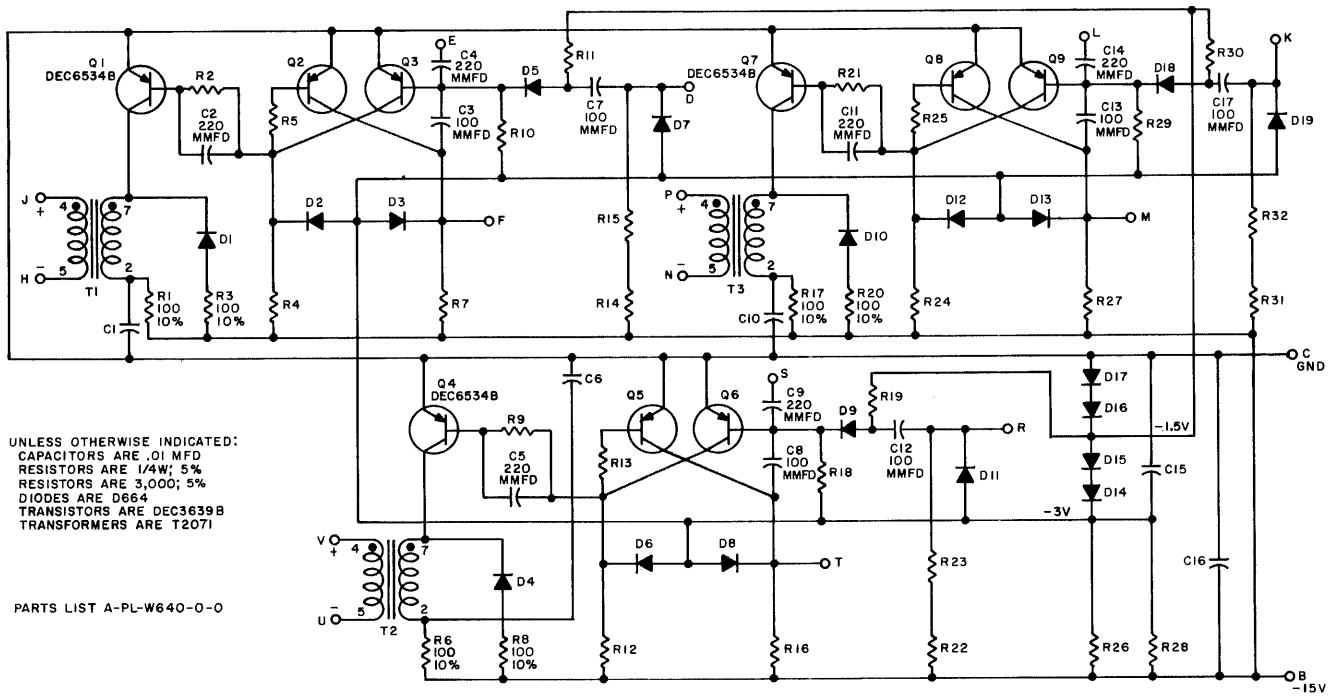
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

C-CS-W103-0-1 Device Selector



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D664

B-CS-W612-0-1 Pulse Amplifier



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01 MFD
RESISTORS ARE 1/4W; 5%
RESISTORS ARE 3,000; 5%
DIODES ARE D664
TRANSISTORS ARE DEC3639B
TRANSFORMERS ARE T2071

PARTS LIST A-PL-W640-0-0

B-CS-W640-0-1 Pulse Output Converter

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